What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming a semiconductor device, comprising the steps of:

forming a conductive layer over an insulating layer;

forming a metal layer over said conductive layer;

forming a protective layer over portions of said metal layer, leaving other portions of said metal layer exposed; and

electropolishing said exposed portions of said metal layer.

2. The method of claim 1, wherein said metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

3. The method of claim 2, wherein said metal layer contains a noble metal.

4. The method of claim 3, wherein said metal layer is a platinum layer.

5. The method of claim 4, wherein said platinum layer is formed by deposition to a thickness of approximately 50 to 300 Angstroms.

6. The method of claim 5, wherein said platinum layer has a thickness of approximately 100 Angstroms.

7. The method of claim 1, wherein said conductive layer is formed of a material selected from the group consisting of tantalum, tantalum nitride, titanium and titanium nitride.

8. The method of claim 1, wherein said conductive layer is formed by deposition to a thickness of approximately 100 Angstroms.

9. The method of claim 1, wherein said protective layer is a photoresist layer.

10. The method of claim 1, wherein said electropolishing leaves portions of said conductive layer exposed, said method further comprising the step of removing said exposed portions of said conductive layer.

11. The method of claim 10 further comprising the step of removing said protective layer.

12. The method of claim 1 further comprising the step of forming an opening into said insulating layer, said conductive layer, metal layer and protective layer being formed in said opening.

13. The method of claim 1, wherein said metal layer forms a lower capacitor electrode of said semiconductor device.

14. A method of forming a lower capacitor electrode on a semiconductor substrate, comprising the steps of:

forming a first opening into a first insulating layer provided over said semiconductor substrate;

forming a polysilicon plug in said first opening;

forming a second insulating layer over said polysilicon plug and said first insulating layer;

forming a second opening into said second insulating layer over said plug;

forming a conductive layer in said opening and over at least a portion of said second insulating layer;

forming a metal layer over said conductive layer;

forming a protective layer over portions of said metal layer, leaving other portions of said metal layer exposed; and

electropolishing said exposed portions of said metal layer.

15. The method of claim 14, wherein said metal layer contains a material selected from the group consisting of metals, noble metal alloys and noble metal oxides.

16. The method of claim 15, wherein said metal layer contains a noble metal.

17. The method of claim 16, wherein said metal layer is a platinum layer.

18. The method of claim 17, wherein said platinum layer is formed by deposition to a thickness of approximately 50 to 300 Angstroms.

19. The method of claim 18, wherein said platinum layer has a thickness of approximately 100 Angstroms.

20. The method of claim 14, wherein said conductive layer is formed of a material selected from the group consisting of tantalum, tantalum nitride, titanium and titanium nitride.

21. The method of claim 14, wherein said conductive layer is formed by deposition to a thickness of approximately 100 Angstroms.

22. The method of claim 14, wherein said protective layer is a photoresist layer.

23. The method of claim 14, wherein said electropolishing leaves portions of said conductive layer exposed, said method further comprising the step of removing said exposed portions of said conductive layer.

24. The method of claim 23 further comprising the step of removing said protective layer.

25. The method of claim 14, wherein said lower capacitor electrode is part of a container capacitor.

26. The method of claim 14, wherein said lower capacitor electrode is part of an MIM capacitor.

27. The method of claim 14, wherein said lower capacitor electrode is part of an MIS capacitor.

28. The method of claim 14, wherein said lower capacitor electrode is part of a ferroelectric capacitor.

29. A semiconductor device comprising:

a substrate; and

an electropolished patterned metal layer provided over said substrate.

30. The semiconductor device of claim 29, wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

31. The semiconductor device of claim 29, wherein said electropolished patterned metal layer contains a noble metal.

32. The semiconductor device of claim 31, wherein said electropolished patterned metal layer is a platinum layer.

33. The semiconductor device of claim 32, wherein said platinum layer has a thickness of approximately 50 to 300 Angstroms.

34. The semiconductor device of claim 33, wherein said platinum layer has a thickness of approximately 100 Angstroms.

35. The semiconductor device of claim 29, wherein said electropolished patterned metal layer forms a lower capacitor electrode of said semiconductor device.

36. A memory cell comprising:

an electropolished patterned metal layer provided over a semiconductor substrate;

a transistor including a gate fabricated on said semiconductor substrate and including a source/drain region in said semiconductor substrate disposed adjacent to said gate; and

a capacitor including an electrode, said electrode having a surface aligned over said source/drain region.

37. The memory cell of claim 36, wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

38. The memory cell of claim 37, wherein said electropolished patterned metal layer contains a noble metal.

39. The memory cell of claim 38, wherein said electropolished patterned metal layer is a platinum layer.

40. The memory cell of claim 39, wherein said platinum layer has a thickness of approximately 50 to 300 Angstroms.

41. The memory cell of claim 40, wherein said platinum layer has a thickness of approximately 100 Angstroms.

42. The memory cell of claim 36, wherein said electropolished patterned metal layer forms said electrode of said capacitor.

43. The memory cell of claim 36, wherein said electrode is a lower capacitor electrode.

44. A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said integrated circuit and processor comprising an electropolished patterned metal layer provided over a substrate.

45. The processor-based system of claim 44, wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

46. The processor-based system of claim 45, wherein said electropolished patterned metal layer contains a noble metal.

47. The processor-based system of claim 46, wherein said electropolished patterned metal layer is a platinum layer.

48. The processor-based system of claim 47, wherein said platinum layer has a thickness of approximately 50 to 300 Angstroms.

49. The processor-based system of claim 48, wherein said platinum layer has a thickness of approximately 100 Angstroms.

50. The processor-based system of claim 44, wherein said electropolished patterned metal layer forms a lower capacitor electrode of said semiconductor device.

51. The processor-based system of claim 44, wherein said integrated circuit is a memory module.

52. The processor-based system of claim 51, wherein said memory module is a DRAM memory.

53. The processor-based system of claim 51, wherein said memory module is a SRAM memory.

54. The processor-based system of claim 51, wherein said memory module is a MCM memory.